ZHEJIANG UNIU-NE Technology CO.,LTD

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U4315/6 Data Sheet

V 1.1

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High Current IO+/- 0.25/0.4A 3-PHASE BRIDGE DRIVER

General Description

The U4315/6 are high voltage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3- phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 V.

Product Summary

V_{OFFSET}	600V max
I_O+/-	0.25 A / 0.4A
VOUT	10~20V
$VCC_{on/off}$(typ.)	8V & 9V
Deadtime(typ.)	200ns
Work Tem	-40 ~150 ℃

Key Features

- Floating channel designed for bootstrap operation Fully operational to +600 V
- Tolerant to negative transient voltage
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- Cross-conduction prevention logic
- Low side output out of phase with inputs. High side outputs out of phase
- 3.3 V logic compatible
- Lower di/dt gate drive for better noise immunity
- Externally programmable delay for automatic fault clear
- All parts are LEAD-FREE

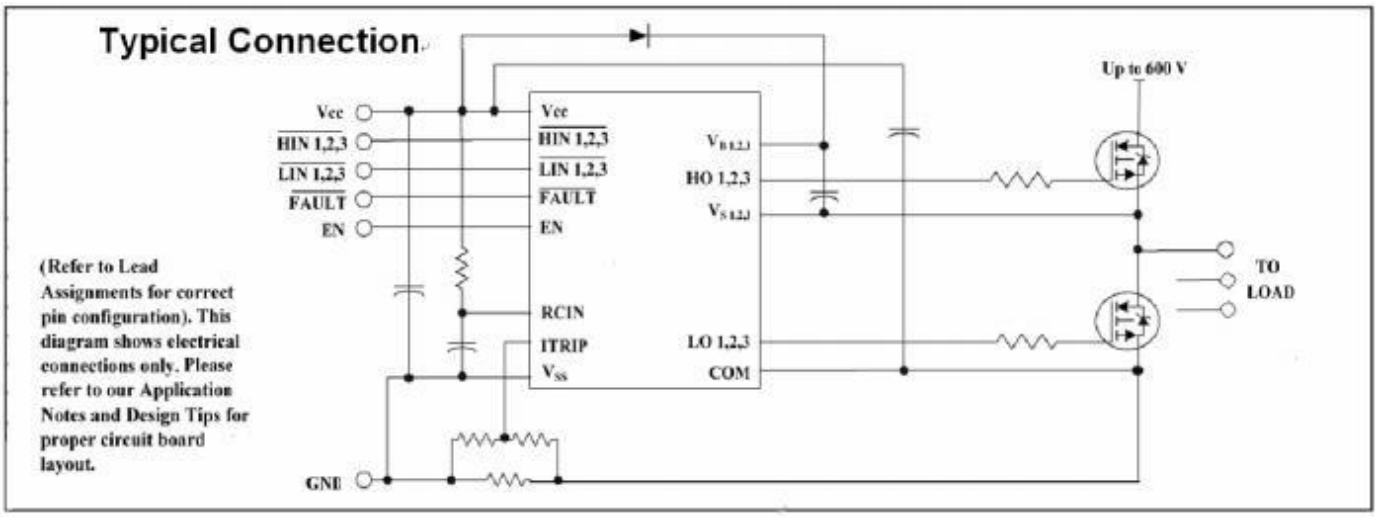
Applications

- 3-phase motor driver
- DC - AC inverter

Package

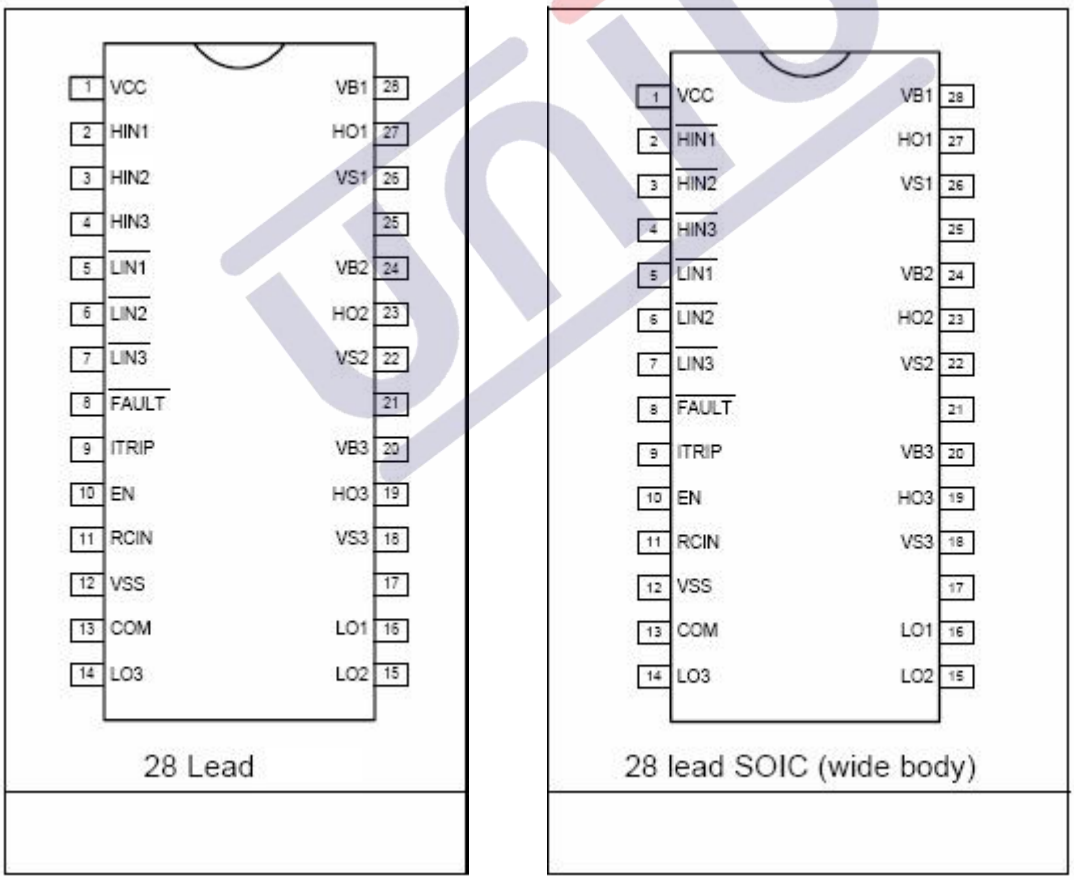
28-Lead SCIC(W)

Typical Application



Packages

28-lead SOIC



The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absute referenced to COM. The VS offset rating is tested with all supplies biased at 15V differential

Pin Function

Symbol	Description
VCC	Low side and logic fixed supply
VSS	Logic Ground
$\overline{\text{HIN1,2,3}}$ HIN1,2,3	Logic inputs for high side gate driver outputs(HO1,2,3),out of phase Logic inputs for high side gate driver outputs(HO1,2,3),in of phase
$\overline{\text{LIN1,2,3}}$	Logic inputs for high side gate driver outputs(LO1,2,3),out of phase
$\overline{\text{FAULT}}$	Indicates over-current (ITRIP)or low-side undervoltage lockout has occured. Negative logic open-drain output
EN	Logic input to enable I/O functionality. Positive logic, i.e. I/O logic functions when ENABLE is high. No effect on FAULT and not latched
ITRIP	Analog input for overcurrent shutdown. When active,ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time TFLTCLR, then automatically becomes inactive (open-drain high impedance).
RCIN	External RC network input used to define FAULT CLEAR delay, TFLTCLR, approximately equal to R*C. When RCIN>8V, the FAULT pin goes back into open-drain high-impedance
COM	Low side gate driver return
VB1,2,3	High side floating supply
HO1,2,3	High side gate driver outputs
VS1,2,3	High voltage floating supply returns
LO1,2,3	Low side gate driver output

1.版本记录

DATE	REV.	DESCRIPTION
2018/04/19	1.0	First Release
2020/10/19	1.1	Layout adjustment

2.免责声明

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